Amendments to the Specification

Please amend the above-identified application, as follows:

Kindly amend paragraphs [0002], [0012], [0021], [0022] and [0029], as follows:

[0002] "Simultaneous AC Logic Self-Test of Multiple Clock Domains," Rich et al., (Docket No. POU920030172US1), ~~Serial No. _____, co-filed herewith~~Serial No. 10/753,801, filed January 8, 2004.

[0012] FIG. 2 depicts an OPCG configuration in support of internal and asynchronous boundary logic for an exemplary clock domain having N asynchronous boundary interfaces in accordance with an exemplary embodiment of ~~U.S. Patent Application No. _____~~U.S. Patent Application No. 10/753,801, entitled "Simultaneous AC Logic Self-Test of Multiple Clock Domains";

[0021] In accordance with ~~U.S. Patent Application No. _____~~ U.S. Patent Application No. 10/753,801, entitled "Simultaneous AC Logic Self-Test of Multiple Clock Domains," filed concurrently herewith and assigned to the instant assignee, a technique is provided for simultaneous logic self-testing, e.g., LBIST, of internal logic and asynchronous boundary requirements of an IC having a plurality of clock domains. (A particular clock domain refers to a specified oscillator and a specified frequency.) The self-testing may be selectively performed on internal logic or asynchronous boundaries, or any combination thereof, of selectively chosen clock domains, or any combination thereof. ~~U.S. Patent Application No. _____~~ U.S. Patent Application No. 10/753,801, entitled "Simultaneous AC Logic Self-Test of Multiple Clock Domains" is incorporated by reference in its entirety.

[0022] FIG. 2 illustrates an exemplary on product clock generation (OPCG) logic core structure 30 interfacing with N clock domains in accordance with ~~U.S. Patent Application No. _____~~ U.S. Patent Application No. 10/753,801, entitled "Simultaneous AC Logic Self-Test of Multiple Clock Domains," cited hereinabove. OPCG 30 receives commands

from self-test state machine (STSM) 18, or another serially connected OPCG, and provides to asynchronous receive clock drivers 32 a functional clock sequence during normal operation, and a scan clock sequence or capture clock during LBIST testing operation. In the illustrated structure of FIG. 2, each respective first through Nth clock domain has a respective asynchronous receive clock driver 32 associated therewith. In FIG. 2, data lines are represented as solid lines; and control lines are represented as dotted lines.

[0029] FIG. 3 illustrates an exemplary control configuration comprising a hierarchy of command transfer blocks 100, 200 and 300 in accordance with an aspect of the present invention for synchronous self-testing of multiple clock domains on a single chip 102. By way of example only, command transfer block 200 is illustrated as controlling commands to three clock domains 110-112, each clock domain 110-112 respectively being associated with a separate OPCG 120-122, respectively; and command transfer block 300 is illustrated as controlling commands to two clock domains 113-114, each clock domain 113-114 respectively being associated with a separate OPCG 123-124, respectively. Exemplary OPCG's 120-124 comprise structures, such as illustrated in FIG. 2 and described hereinabove, for testing multiple clock domains and asynchronous boundaries in accordance with ~~U.S. Patent Application No. _____~~ U.S. Patent Application No. 10/753,801, entitled "Simultaneous AC Logic Self-Test of Multiple Clock Domain," cited hereinabove.